Group 7 Semiconductor Research

Final Report

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Introduction:

Our project's client is Dr. Chen, an assistant professor in the school of Informatics, Computing, and Cyber Systems at Northern Arizona University. She is the primary investigator of the Semiconductor and Device Research Lab (SDRL) at NAU, where both of the Team 7 members have been undergraduate researchers for two semesters. She was awarded her Ph.D. from the department of electrical and computer engineering at the University of Texas, Austin - where her primary research focus was on that next generation non-volatile memory application for storage class memory and new computing platform. One of the primary research topics of this lab is in the fabrication and characterization of RRAM devices and its use in brain inspired computing. Our capstone project will contribute to the mission of this lab by providing a comprehensive look at the complete process, from fabrication to characterization, of WOx RRAM. Her guidance throughout this process and mentorship on successful research-based projects as well as her technical expertise was exceptionally useful during this project.

The primary focus of this project is to evaluate the use of Tungsten Oxide(WOx) as an active layer in a metal-oxide resistive random access memory (RRAM) device. As this is an emerging type of memory device research is vital in determining effectiveness of materials and improving current design and application. As advances in computing continue to develop the need for fast and reliable memory develops as well, RRAM stands to be the answer to the developing need for machine learning. Therefore, RRAM must be efficient, fast, and reliable. In order to fulfill requirements the team will fabricate, test, and characterize a variety of devices to access necessary metrics. This process will include the fabrication of three dielectric layer thicknesses and five feature sizes to have an array of thickness and feature sizes to access. The goal for the project is to complete fabrication, perform testing, and produce a characterization of each of the thicknesses and feature sizes to provide a holistic view of Tungsten Oxide as an active layer of RRAM devices fabricated via physical vapor deposition machine in a non- clean room academic facility.

Design and Procedure Process:

Our experimental design flow consisted of a three part system with necessary checks throughout. We begin with a research based approach to determine the optimal materials and fabrication method. Once materials and methods are chosen, devices are fabricated to meet device requirements. Simultaneously as

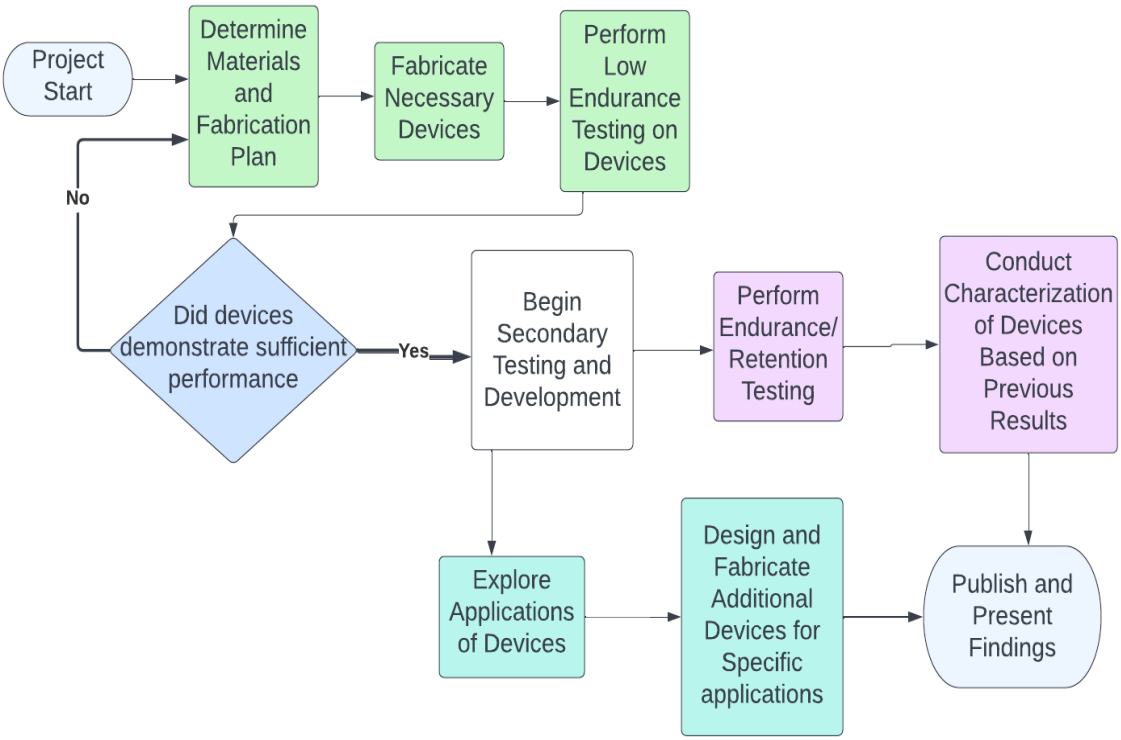


Figure 1: Design Flow Architecture

In following the above design flow we began by fabricating nickel/WO3/nickel devices. Our first device fabricated had the following deposition procedure:

1. Clean Si substrate and vacuum down physical vapor deposition chamber
2. Deposit Nickel onto Si substrate
3. Deposit WO3 onto Nickel coated substrate
4. Break vacuum and place shadow mask
5. Vacuum down physical vapor deposition chamber
6. Deposit Nickel

This device had an extremely low yield, and overall did not demonstrate resistive switching. We theorized the that edge between the active layer (WO3) and nickel top electrode could be causing

issues with our probe technique. We then fabricated three additional devices with the same materials but using a different deposition procedure, it is as follows:

1. Clean Si substrate and vacuum down physical vapor deposition chamber
2. Deposit Nickel onto Si substrate
3. Deposit WO3 onto Nickel coated substrate
4. Break vacuum and place shadow mask
5. Vacuum down physical vapor deposition chamber
6. Deposit nickel top electrode

As shown in the figure below, the reorder of steps allowed us to eliminate the edge of the active layer and top electrode; this procedure created an “edgeless” device.

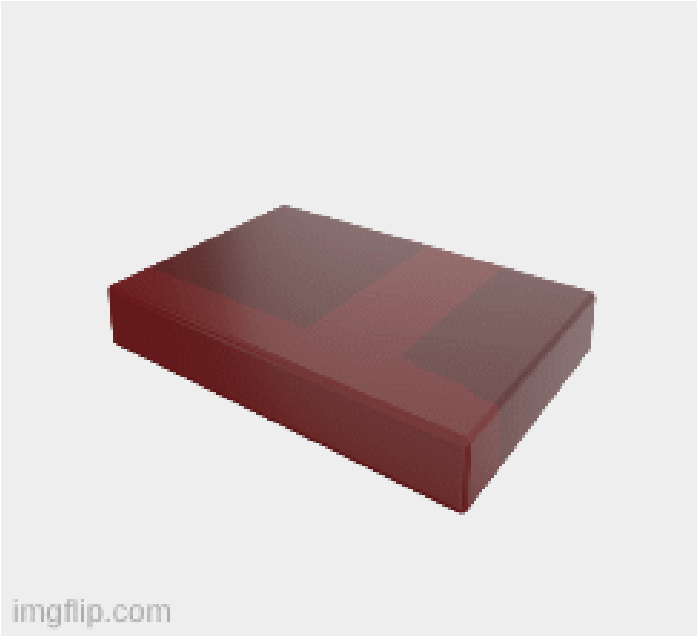


Figure 2: Animation of the “edgeless” nickel/WO3 deposition process

Despite this change, none of these devices had a sufficient yield. Furthermore, the edgeless device design made probing and therefore electrical testing difficult. It was hard to ensure proper probe tip placement, and the method we used eventually led to damage to a probe tip and therefore could no longer be supported. This hurdle made the results we obtained unreliable and often required us to probe the same device multiple times to ensure we were getting accurate results and measuring the correct things. After exhaustive tests of all three active layer thickness of the nickel/WO3 devices we determined that the yield was not sufficient to move forward. These results will be further shown in the prototypes section later on. We then used the testing results as well as research to determine our next electrode choice. We decided upon Indium Tin Oxide(ITO), as research showed it had suitable properties. The device fabrication procedure is as follows:

1. Clean ITO coated glass slide and vacuum down physical vapor deposition chamber
2. Deposit WO3
3. Break vacuum chamber and place shadow mask
4. Vacuum down physical vapor deposition chamber
5. Deposit ITO top electrode

This procedure differers in a few key ways. Our bottom electrode is pre-coated and therefore eliminates one deposition and possibly helps to decrease impurities occurring during deposition as we are not in a clean room setting. This procedure also produces an “edged” device which makes probing easier and more effective. The procedure can be seen below.

Figure 3: Animation of ITO/WO3 “edged” device deposition process

These devices had a significantly better yield. This enabled us to move past the low level endurance testing and move on to the more performance based testing, namely the endurance and retention testing. From there we also were able to do optical characterization of the devices and design additional novel applications. These findings will be discussed further in the final design and results section.

Prototypes:

The prototypes for this project consisted of two of the nickel/WO3 devices. The findings from these prototypes were essential in the decision to move away from the nickel electrode. The devices fabricated and tested for this procedure were the 100nm active layer device and the 20nm active layer device.

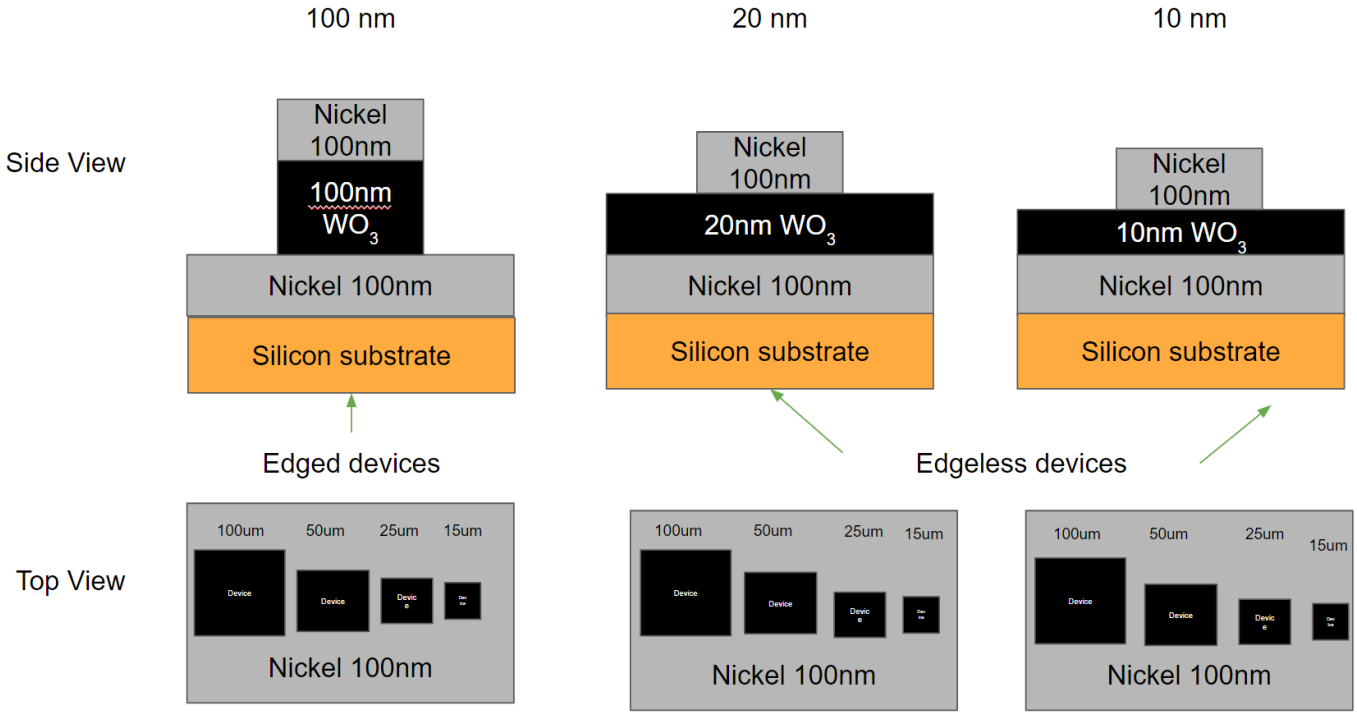


Figure 4: 100 nm Ni/WO3 Device schematic

For our first round of device the basic device structure is unchanged between the three different devices. It is a metal-insulator-metal (MIM) structure with symmetric electrodes made of nickel. The insulator layer is a transition metal oxide known as Tungsten Oxide (WO3 or WOx). The project design states that we will make three different RRAM samples with three different Tungsten Oxide layer thicknesses, shown in the side view figure above. These thicknesses are 100 nanometers (nm), 20 nm, and 10nm. Additionally, by use of a shadow mask we fabricated four different device feature sizes, 100 micrometer (um), 50 um, 25 um, and 15 um, shown above in the top view figure.

The first prototype fabricated was the 100nm WOx thickness device. Prior to fabricating the 100nm device we ran into issues during several depositions. My first attempt at deposition failed due to the QCD thickness sensor failure. This caused the WOx layer to have an unknown thickness. After fixing the sensor and doing maintenance on the deposition system I attempted to fabricate the 10-nanometer device. Quickly, I learned that electron beam deposition of transition metal oxides was difficult as they evaporate at an extremely fast deposition rate (~nanometers/per second) and I accidentally deposited too much WOx on the silicon target. In the design section of this document I outline how I solved this problem to fabricate the 100 nanometer device.

After fabricating the 100 nm preliminary testing was performed to see the results of the fabrication. First, non-volatile memory behaviors were demonstrated in the 100 nanometer device, as shown in the figure below.

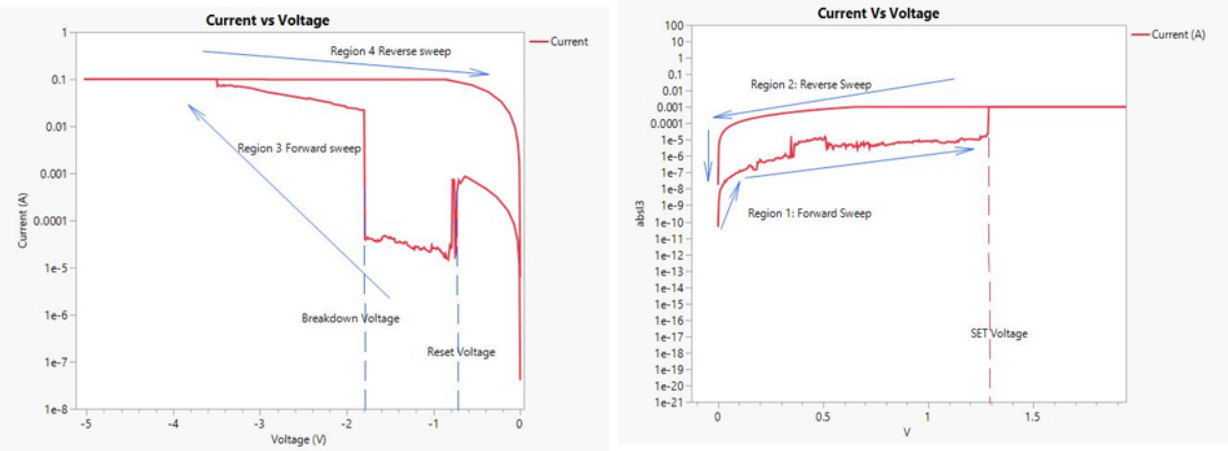


Figure 5: I-V curves for the 100 nm Ni/WO3 Device

First, to describe the switching sweeps refer to regions 1,2,3 and 4 drawn on the figure . First, in region 1 a positive voltage is swept forward from 0 Volts to 2 Volts with a compliance current limit (CCL) set to1mA. During this forward positive sweep (SET sweep) the current will rapidly jump several orders of magnitude at the SET voltage, in this case 2 orders of magnitude. The SET current in this device hits the 1mA CCL, indicating that this device, and likely most devices, suffer from high switching power. Then, in region 2, the reverse sweep begins at 2 Volts until it is swept back to 0 Volts. Because the SET process occurred, the current was higher on the reverse sweep, indicating a low resistance state (LRS) on the order of kilo-Ohms. Next, in region 3, the negative voltage sweep begins at 0 Volts and ends at -5 Volts. In region 3 you will see 2 distinct features, one is the rapid drop in current occurring at ~1 Volt, this is called a RESET. Once the sweeping voltage is at the RESET voltage the device enters a high resistance state (HRS) on the order of hundreds of kilo-Ohms to mega-Ohms. At negative 2 volts, a rapid increase in current occurs. Dr. Chen and I have confirmed that this second jump in current is dielectric breakdown, which is a permanent deformation of the active layer. This permanent dielectric breakdown forms a low resistance channel, and the device will forever be a low resistance, you can think of this as a “broken” memory cell. To prevent dielectric breakdown the RESET sweep, stop voltage must be reduced to some value between -1 and -2 Volts.

The most important result from the 100 nm prototype was the device yield. It was found during the prototype testing that 90% of the devices were in a pristine low resistance state. Pristine low resistance state means that we have never applied voltage to the device and upon reading the resistance it is between 10 and 500 ohms. This prototype result caused us to change some of the fabrication procedures to try and increase the device yield. The first of these changes

was decrease the vacuum chamber pressure from 9*10^-6 Torr down to 6.0 *10^-6 Torr, as it was believed it would decrease the number of defects in the active layer. As well, we moved from an “edged” device to an “edgeless” device with some belief that it would also mitigate defects in the active layer.

The vast majority of devices were found in a pristine low resistance state. They all have a current-voltage curve which looks like the figure above. The sweep currents are on the order of milliAmperes which shows how it is in a very low resistance state. As well, these devices do not demonstrate a memory window after the first cycle, which means it is in a dielectric breakdown state. The yield of devices in each state for the 100 nm sample is shown in the pie chart below.

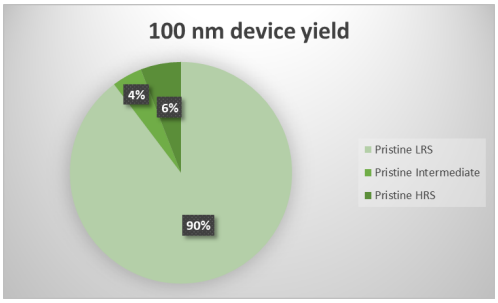
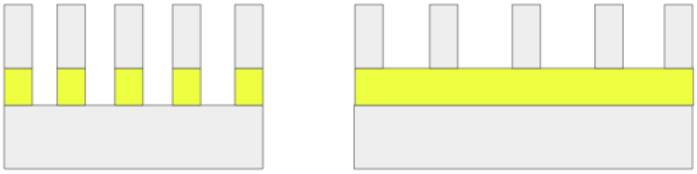


Figure 6: Yield of 100 nm Ni/WO3 Device

As a consequence of this pie chart, our team decided to decrease the vacuum pressure for the 10 nm and 20 nm devices. As well, we fabricated edgeless 10 nm and 20 nm devices to improve the yield. We have two main hypotheses as to why there are so many failed devices:

1. Poor fabrication conditions (PVD no clean room) leads to high density of defects (Oxygen vacancies).
2. Edged devices have a high density of defects.

The second prototype was the 20nm WOx thickness devices. As stated above we switched to the edgeless device, as demonstrated in figure 6, as well as lowering the vacuum pressure.



a. Edge Device, shadow mask applied for active layer and top electrode deposition.

b. Edgeless device, shadow mask only applied for top electrode deposition

Figure 7: Schematic of edge vs edgeless device

This device was necessary to fabricate in order to test our abilities to reduce deposition rate of the oxide layer in order to achieve the 20 nm and 10 nm thicknesses needed. The 20 nm was chosen because it provided more room for error whilst still allowing us to test this process. In order to test this device the probe tip (which is magnitudes larger in the z axis than our device) is poked through the active layer in order to reach the bottom electrode. As well, this device had several fabrication changes made and should not be directly compared to the 100 nm device, as there are simply too many variables to decouple for accurate analysis to be made. However, this device can be accessed on its own. In this device we initially believed we had found that we were able to demonstrate non-volatile memory windows and that the device did not go into dielectric breakdown. However, upon further inspection of the probing procedure we discovered that due to the fabrication changes our results were inaccurate. The new probe method was actually causing one of the probe tips to act as an electrode and therefore we were unable to prove resistive switching with the approach. We changed probing methods, and with this change we were not able to demonstrate resistive switching. We also encountered numerous issues with testing the device as the structure made probing very difficult and led to damage to the probe tip. These findings confirmed that we needed to decide upon a different electrode scheme to accurately and efficiently produce and test our memory devices.

Final Design:

Final Design - Fabrication:

Our ITO/WO3 devices were the final iteration of device design. These devices differed from the Ni/WO3 devices in both material and fabrication methods. These were “edged” devices, and therefore provided a much easier testing set up. The fabrication procedure is shown below. Additional information can be found in Appendix A.

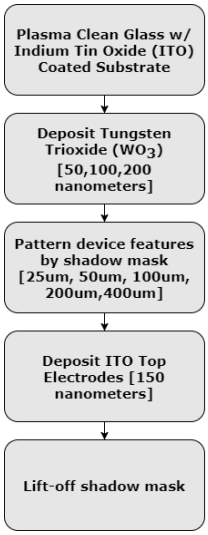


Figure 8: ITO/WO3 Device Fabrication Flow chart

This fabrication process produced all of the memristors analyzed in the results section and we confidently believe this process is able to produce quality memory at an academic level. This procedure allows for memory to be created in a non-clean room environment at a relatively inexpensive cost and with relative ease of use. The physical structure of these devices is shown in the figures below.

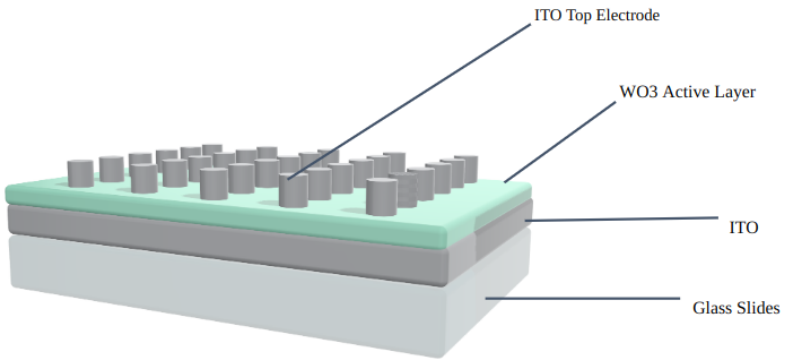


Figure 9: Final Device Wafer Level Schematic

Figure 10: Final Design Device level schematic

These devices were easily testable with our probe station and produced quality results, as shown in the results section.

Final Design - Testing:

The final test set-up is shown below. These devices did not cause any damage to the probe tips and responded well to electrical stimulus with fairly consistent results from working devices. As with all devices, yield was not 100%, it was, however, much higher than the Ni/WO3 devices and enabled sufficient data for further analysis. Detailed testing procedure given in user manual.

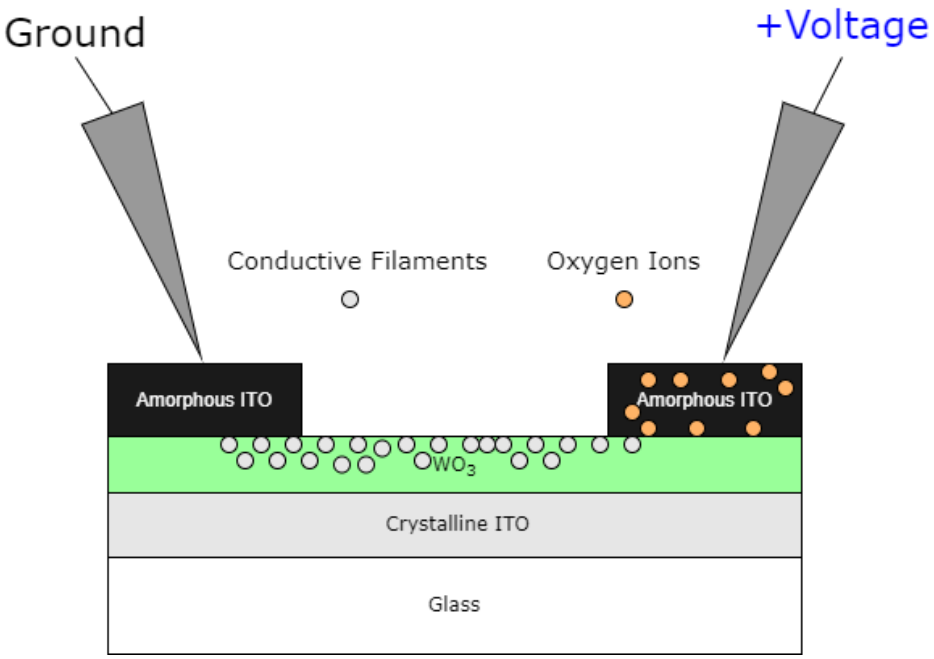


Figure 11: Final Device Structure with Physical Model of Testing

Results:

Requirements:

Table 1: Project Requirements with Color Coded Testing Requirements and Status

Type of Test	Status	Req #	Requirement
Fabrication		1	Top electrode thickness must be greater than 100nm but less than 200nm.
		1.1	1. Active Layer must be fabricated at different thicknesses: 10nm 20nm 100nm thicknesses.
Material		2	Electrode material must be Nickel or ITO
		2.1	Active layer must be WO3
		2.2	All material properties may be verified with Energy Dispersive Spectroscopy- line scan.
Deposition		3	Vacuum Pressure must be below 9.99 *10^-6 Torr when doing vapor deposition.
		3.1	Deposition rate must be recorded.
		4	Multiple devices must be tested.
		4.1	Different feature Sizes
		4.1.1	100um, 50um, 25um
Electrical		4.2	For each feature size and thickness 20 devices must be tested, and data must be compared to evaluate Device to Device (D2D) variation
		4.3	For each feature size and thickness 20 switching cycles must be performed to evaluate cycle to cycle (C2C) variation.
		4.4	Memory Performance Testing
		4.4.1	I-V Curves
	*	4.5	MLC Testing
	*	4.6	Endurance testing 10^9 Cycles
	*	4.7	Retention Testing 10^12 seconds (extrapolated)
Characterization		5	Characterization Requirements
	*	5.1	Fit to mathematical conduction models
	*	5.2	Extraction of barrier height
	*	5.3	COMSOL Model
Optical Test		6	UV-Visible Spectroscopy

		6.1	UV-Visible spectroscopy on ITO devices at each thickeness at each stage of the fabrication
		6.2	Annealing of ITO to induce transparency in the visible wavelengths
		6.3	Extraction of band gap from absorbance

The color code for requirements is as follows: green indicates that testing has been completed and if applicable, the device passed. Black indicates testing has not been completed, typically due to lack of required materials/device or testing being deemed unnecessary. A * indicates testing we would like to perform in the future but unfortunately fell out of the scope and time limits of this project.

Testing Results:

Testing is a major component of this project. The majority of testing is carried out during the low endurance cycling stage - as this provides the most insight into the functionality and yield of the fabricated devices. There is also significant testing that must be performed to determine device performance and to properly characterize the device. The flow chart below shows how testing fits into the overall experiment procedure.

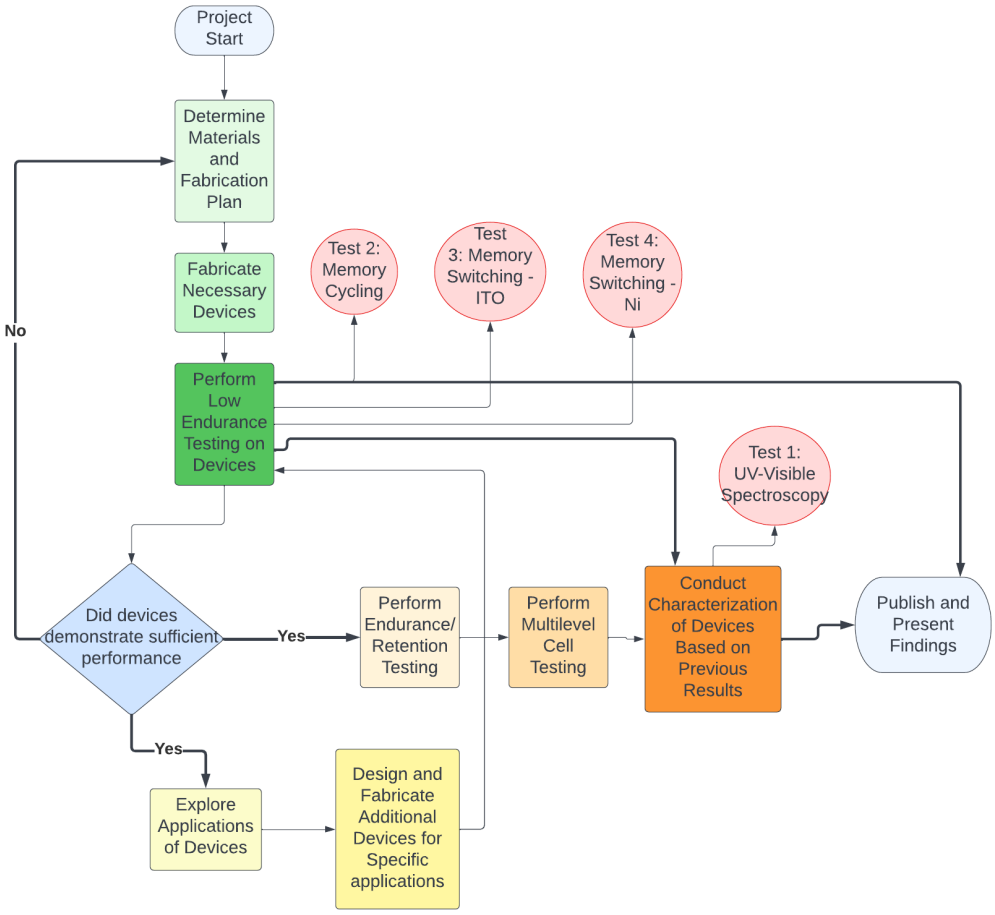


Figure 12: Project Architecture with Indicated Testing Procedures

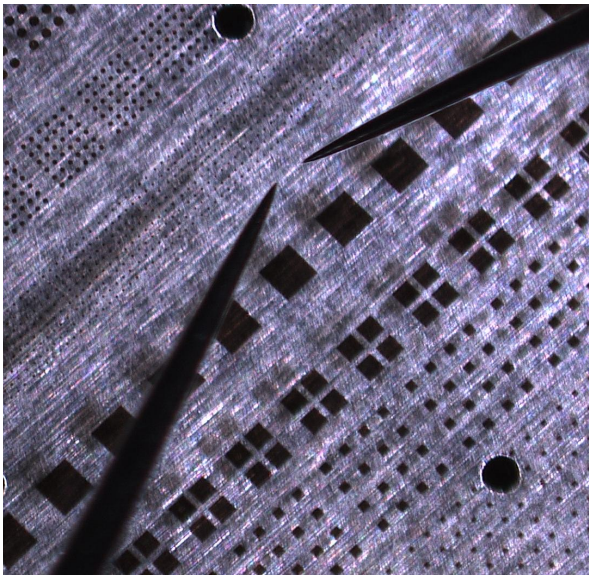


Figure13: Top-Down View from Probe Station CCD. This view shows (from top to bottom) the 50um and 25 um Circle, and the 400 um, 200um, 100um, and 50um square feature sizes

This testing procedure is what we used to determine validity of device structure and also produced our final device results. Below is a highlight of our most important testing results. Below is a specific breakdown of the testing architecture applied to our devices.

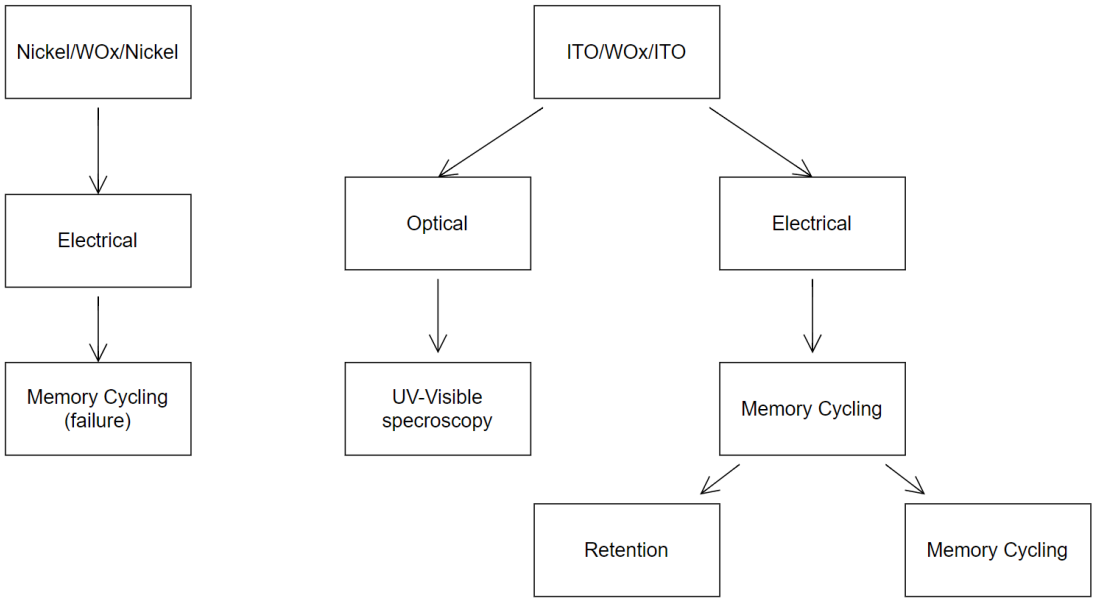


Figure 13: Applied Testing Architecture

Major Test Results:

Types of Test:

1. Unit Test Step-By-Step: ITO/WOx/ITO Memory Cycling
    a. 20 memory switching cycles.
2. Unit Test Step-By-Step/Matrix: Ni/WOx/Ni Memory Cycling
3. Unit Test Matrix: ITO/WOx/ITO memory cycling at different thicknesses
    a. 20 devices at each thickness (50 nm ,100 nm ,200 nm)
4. Unit Test Matrix: ITO/WOx UV-Visible spectroscopy at different thicknesses

Major Tests:

1. ITO/WOx/ITO memory cycling (Step by step and Matrix)

This was the primary form of testing for our project, and thus most of the results come from this type of testing. The results are shown in the Appendix figures 6 through 11. Figure 6 is a typical memory cycle where forming, set, and reset are shown, this is the step by step test. First the device is put through a forming sweep with a high voltage stress with a current limit at 5mA in which the device enters a low resistance state. Then, a negative voltage sweep to -6V is performed where the device transitions back to a high resistance state. This first reset stop voltage of -6V is different from subsequent reset cycles where the stop voltage was -3V. Finally, the set sweep of 2V with a current limit at 5mA switches the device back to the low resistance state.

2. UV-Visible spectroscopy of ITO/WOx

This was originally a matrix test in which the spectrum was taken for the three different thicknesses. However, the results were all the same so the 50nm spectrum was used for the analysis.

Analysis of Results:

It is evident that the resistance states have a high degree of variation. No noticeable trends are seen in the resistance states versus thickness other than the fact that the 50nm states have the highest variation. This leads to figure 9 memory window plot (memory window is the difference between high resistance and low resistance state). The highest memory window is seen in the 50 nm device. The trend shows that the memory window decreases with increasing WOx thickness. The set/reset voltage box plot has similar variation to the resistance states, but with the trend that the reset voltage decreases with increasing WOx thickness. A key performance parameter is that the majority of the set/reset voltages are between +1V and -1V.

Using this testing results data on the ITO/WO3 devices, the thickness of the WOx, and Bouguer-Lambert law I was able to extract the absorption coefficient. Using the absorption coefficient I was able to make a Tauc Plot in which the x-intercept of the linear region is the energy band gap (3.3eV) which is typical for WOx deposited by physical vapor deposition at room temperature.

It is evident that the devices have no resistive switching in the Ni/WO3 devices. We did not expect this result, but hypothesize that the lack of switching is due to the lack of an "oxygen reservoir" electrode. Because both electrodes are nickel it is possible that after forming, the oxygen ions and nickel are creating a nickel oxide and preventing Reset from ever occurring due to lack of free oxygen.

Device Results:

First, the oxygen ions and corresponding vacancies are generated through a high voltage stress called electroforming, which leaves the device in the low resistance state (LRS). Next, the first reset voltage sweep (-6V) occurs and the oxygen returns to rupture vacancies, leaving the device in the high resistance state (HRS). Then, the set sweep (+2V) occurs, and liberated oxygen drifts to the ITO electrode once again, returning the device to LRS. The subsequent reset cycles are -3V sweeps. Finally, this memory switching process is repeated for 20 cycles. This result can be seen below.

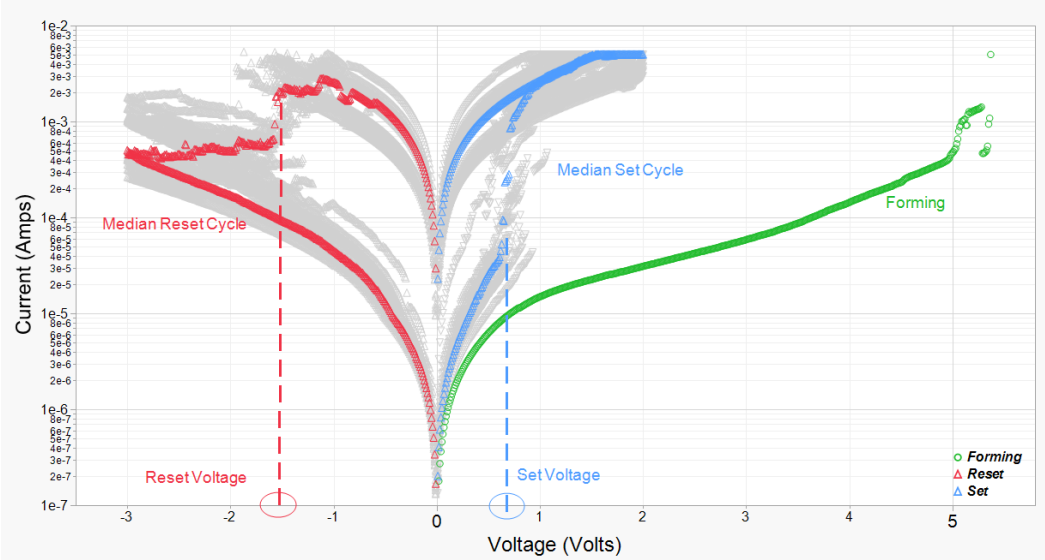


Figure 14: Memory Cycle for ITO/WOx/ITO

This is a typical "butterfly curve" that is associated with memristors, which is the I-V curve. The forming voltage is noted along with the set and reset curve. It is the space in between that makes up the memory window. This is our proof of resistive switching with a measurable memory window. Indicating a successful fabrication of a memristor.

The below graph shows some key characteristics of our devices. These plots give us an overview of all of our fabricated devices as a whole. Some key takeaways are the overlap of high and low resistance values in the 200nm devices. This result indicates that this thickness level is not appropriate, as an overlap makes for an ambiguous result and therefore discredits the device for use. The largest memory window is seen in the 50 nm device, which on its own would indicate

that this is the best of the produced devices, which would correspond well to the research of these devices. However, this device also has the highest variation in the high resistance state. This leads to a need for further investigation of these devices in order to optimize, this will be covered in greater detail within the future work section.

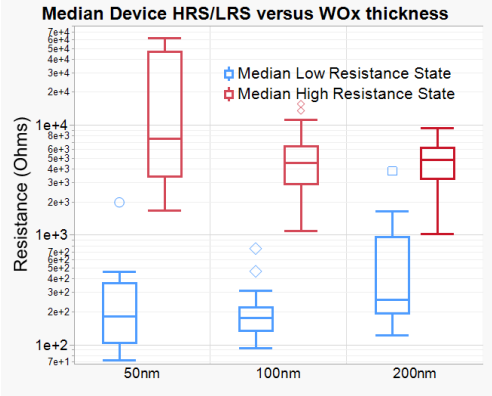


Figure 15: Resistance States versus Thickness

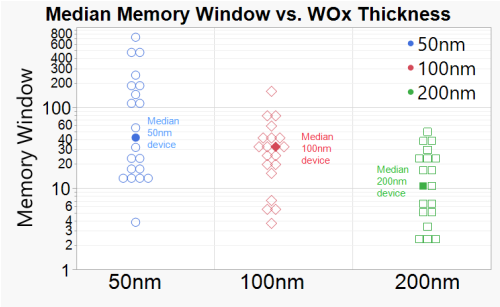


Figure 16: Memory Window versus Thickness

Another key characteristic of memory devices is the set and result voltages. Here we can see the median for all devices lie within an approximate (+/-) 1 volt range. This is promising for low power devices.

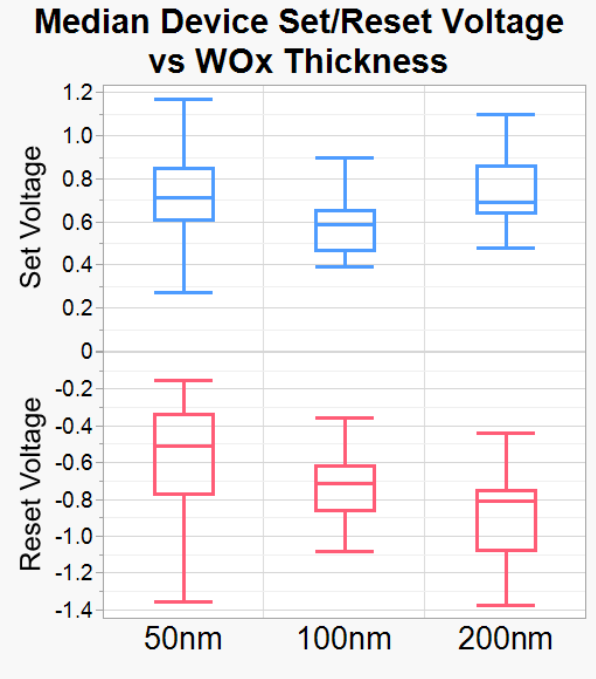


Figure 17: Operation Voltages versus thickness

The figures below show the results of our performance and reliability based testing. This gives us information beyond yield and basic device analysis. It can be see that for 200 cycles, which is notably below industry standard for endurance testing but does provide a 10x larger cycling than our low endurance testing, that high and low resistance states remain fairly consistent. This is promising as it demonstrates these devices have the capacity to be used heavily for writing and rewriting memory. This is a necessary feature for an industrially produced device. Our findings give merit to the use of memristors in further applications. Our retention results are less optimal. It can be seen that the high resistance state begins to vary after one hour. As these devices are non-volatile memory devices, which in industry have a retention rate of approximately 10 years, this is not ideal. However, this is a common issue for academically created devices, especially those created in a non-cleanroom environment. We would like this to be investigated further in future works to increase optimization of these devices at an academic level.

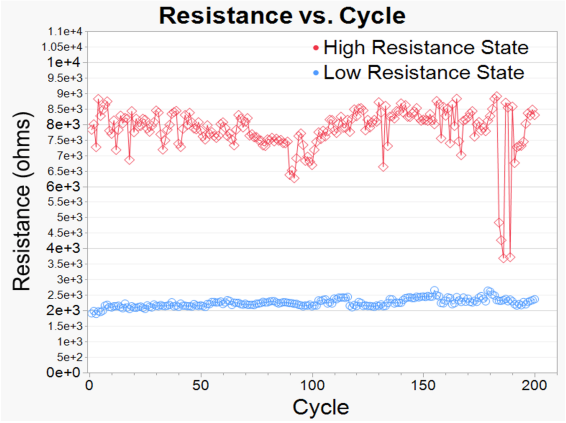


Figure 18: Endurance Testing

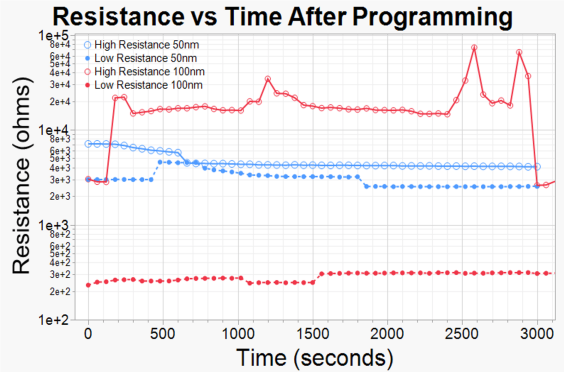


Figure 19: Retention Testing

Optical Characterization:

The optical characterization was able to provide us with the band gap energy of 3.3 eV. This is a typical band gap for a memristor. Information on procedure and equipment can be found in Appendix B.

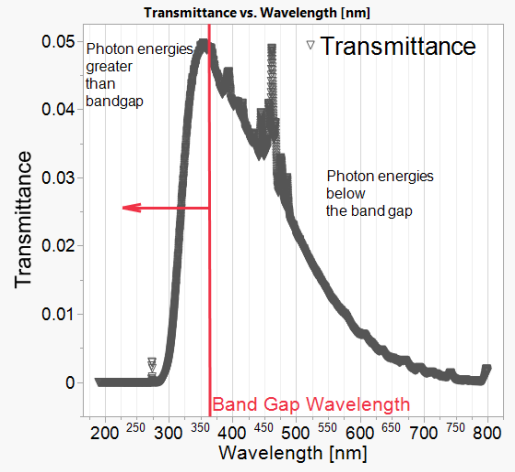


Figure 20: Transmittance Spectra (UV to Visible)

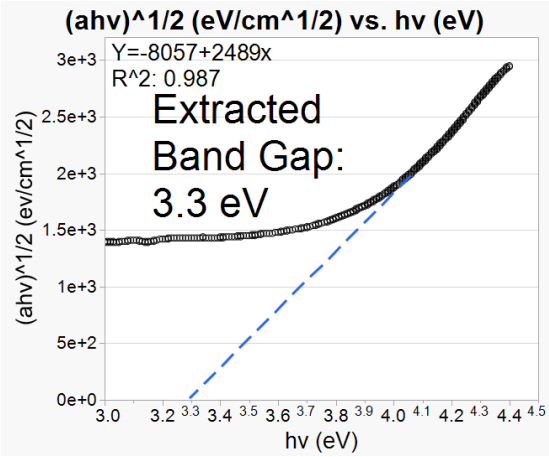


Figure 21: Tauc Plot with extracted band gap

Future Work:

Additional Research:

While we feel like our project is complete as is and that we were able to provide meaningful insight into the use of WO3 as an active layer as well as providing an appropriate electrode material. There is still much work to be done in further understanding the mechanism of these devices as well as optimizing these devices, especially at an academic level. Two of the main research efforts we would like to see include comparing planar ITO/WOx/ITO to vertical amd utilizing X-ray photoelectron spectroscopy and Energy Dispersive Spectroscopy to analyze material properties. We would also like to further investigate the poor retention rate to see if there are changes that could be made to improve this metric.

Memory Applications:

Another avenue of future work we would like to investigate is the real-world applications we could use this memory and fabrication technique on. One promising application of these memory devices is flexible memory. We have fabricated a flexible substrate, which enables the use of our technique for a planar deposition but will not be bound by a rigid substrate. This provides an opportunity to develop onboard memory for flexible electronic devices. The proposed model device model is shown below.

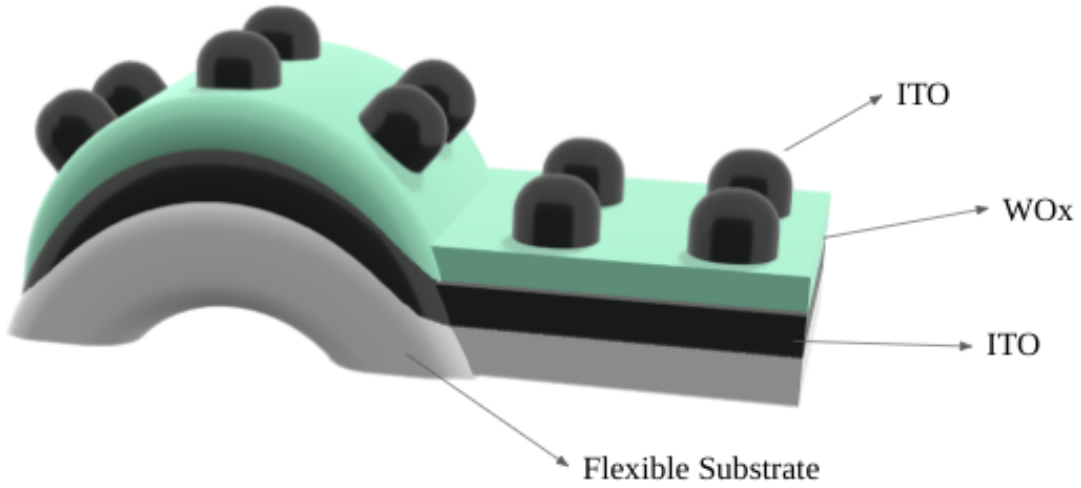


Figure 22: Proposed Flexible memory design

During our work on this project we researched, designed, and fabricated a flexible substrate, as shown below. This substrate was able to bend and flex, and be easily transferred to a clear flexible bandage, which would enable this device for possible medical sensor usage. Furthermore, we were able to test the substrate in the PVD and it showed no out-gassing, which means the same technique used with the rigid surfaces could be used with this device.

Figure 23: Flexible Substrate

Overall, we think that memristors hold great potential as the next industry standard memory device and we are excited to see the future of these types of devices.

Conclusion:

In short, for our capstone project Team 7 has embarked on fabrication, testing, and characterization of RRAM devices with a WOx active layer. This work is being done in conjunction with the efforts led by our client, Dr. Chen of NAU and her lab, SDRL. Similarly to the efforts of the SDRL, we hope to promote the research and development of these emerging memory devices that have great potential in the world of machine learning. In our first semester we have completed three out of four device fabrications. During our initial testing efforts we discovered a potential defective practice and devised a design change that we hope to prove will increase yield. This leads to another metric in which we can analyze and report on: the edge vs edgeless effect. This demonstrates our need to have a feedback loop on our fabrication - test - characterization process. We were able to obtain important information on our fully fabricated and function devices, with the most important characteristics being:

1. Set/Reset Voltages of device lie between +/- 1V.
2. Reset voltage is lower for smaller WOx thickness
3. Low resistance states vary around 500 Ohms
4. High resistance states lie near 1.5 kOhm to 10 kOhm.
5. Memory window is 101 -102 .
6. MW decreases with increasing thickness
7. Devices can endure 200 cycles.
8. Devices demonstrate poor data retention over an hour.
9. Absorbance spectroscopy confirms that the band gap is 3.3eV.

This process did not come without challenges though. We believe that these challenges provided us with great insight into research experimental design as well as into the devices physics of memristors. The main lessons learned from this process are the importance of building in more time for fabrication. We initially believed we could fully fabricate three device thicknesses in only a few weeks but we found this was very difficult to do. One major contributor to this delayed process was the equipment we had to use. Our deposition machine failed two times which slowed progress as well as the maintenance it required as entire weeks progress were halted due to foil replacement. Additionally, we learned that for our first round of devices the device structure prohibited successful probing, as probing edgeless devices twisted the probe tip so we couldn't test with that method; this meant that getting a good ground probe by poking through the WOx made testing procedure arduous and uncertain. Most importantly we learned that our experiment design structure halted productivity. After evaluation we determined that we should have thoroughly tested the first device, which should have been the most ideal device, i.e the thinnest active layer after fabrication and before attempting to fabricate any additional devices.

User Manual (How to reproduce results):

Introduction:

We are pleased you wish to further the research efforts began by Group 7, Semiconductor Research. We hope that you find the following steps easy to follow and aid you in your research efforts. There is strong need for academic and industry level research into emerging memories if we wish to be able to continue device scaling at current level. While memristors have a long history of investigation they are currently not the industry standard. While one major reason for this is the massive undertaking of converting a fabrication facility that makes the current technologies the end of the transistor based memory device is growing near and it is our belief that RRAM has the capacity to be the future's answer to fast, reliable, easy to manufacture non-volatile memory. We perform this research to best prepare for when society needs this innovative memory. It is our goal to showcase that RRAM fabrication can be done in a low cost way. We hope that this provides incentive to not just those in industry but to other university level researchers to pursue creating the next best memory device. In our project we have used this procedure to produce working memristors in a non-clean room setting. This procedure was relatively inexpensive, as the material use was very limited, and compared to industrial practices the equipment is extremely inexpensive and is available at many universities, including NAU. Our memory devices displayed relatively good metrics in the majority of tested areas. A few of our most promising results are:

- Set/Reset Voltages of device lie between +/- 1V.
- Reset voltage is lower for smaller WOx thickness
- Low resistance states vary around 500 Ohms
- High resistance states lie near 1.5 kOhm to 10 kOhm.
- Memory window is 101 -102 .
- MW decreases with increasing thickness
- Devices can endure 200 cycles.
- Devices demonstrate poor data retention over an hour.
- Absorbance spectroscopy confirms that band gap is 3.3eV.

We provide you here with a comprehensive approach to fabricate memristors. We also provide necessary insight into the proper testing procedures needed to understand the memory you create. The objective of this document is to aid your fabrication and test process and hopefully allow you to avoid some of this mistake we made along the way.

Project Design:

While the rest of this document will contain specific examples from our project, we would like to provide specific guidance on how you can best design your experimental flow. To begin we strongly recommend a thorough investigation on which materials you would like to

use. For the electrodes you will need at least one noble metal (non-oxidizing metal). From there you will want to investigate active layers and access your desired outcome. If you are seeking to produce novel devices this is a promising area to introduce novel materials. From there you must determine how to fabricate your devices. If you are using only PVD the majority of your decisions will be on layering. We suggest that you create “edged” devices. That is there is a solid active layer and only the top electrode is patterned. Additionally, we would recommend that your test flow be to fabricate the most theoretically ideal device and fully test it before moving on to other devices. This will give you the most amount of time to redesign your structure and ensure you do not waste any more time than necessary fabricating devices with fundamental issues that will not work.

Fabrication:

Start with an Indium Tin Oxide (ITO) coated glass slides prepared with crystillane ITO. Plasma clean in an Oxygen environment for 5 minutes with Harrick Plasma PDC-32G plasma cleaner. Utilizing an electron beam physical vapor deposition system, vacuum the deposition chamber to a pressure of 10^-6 Torr with the sample mounted in a sample holder. Use Kurt J Lesker company Tungsten Trioxide 99.99% purity pellets in a Molybdenum crucible. Use a filament voltage of 6.5kV and target the corner of the crucible to limit the deposition rate. Keep deposition rate between 0.01 and 0.5 angstroms per second. Deposit the WO3 at 50, 100, and 200 nanometers thickness. After depositing the WOx, you must order a shadow mask from PhotoScientific with feature sizes of 400,200,100,50, and 25 micrometers. The electrodes must be 55 micrometers apart. Place the shadow mask on the sample and secure it with vacuum safe tape. Then place a new ITO crucible with ITO pellets (90%:10% weight ratio) from Kurt J Lesker in the deposition chamber. Use the same electron beam voltage as before to deposit 150nm of ITO electrodes. Lift off the shadow mask and the devices will be complete.

Testing:

Using a Keysight B1500A Semiconductor Device Analyzer and a probe station you can test the device characteristics. First, set the voltage probe down on a 50 micrometer electrode and then place the ground probe on an adjacent electrode. Use the following DC memory cycles:

1. Forming: 7 Volts 5mA compliance current
2. Reset: -6V
3. Set: 2V 5mA compliance current
4. Reset: -3V 20 cycles
5. Set: 2V 5mA compliance current 20 cycles

To perform endurance testing simply do these cycles for 200+ cycles. To perform the retention testing simply leave a device in the high resistance state or low resistance state and do a 0.1 Volt read sweep every minute for an hour.

Conclusion:

We thank you for your desire to continue our research efforts. We hope you found this document a helpful place to begin your project. We wish you a successful project and hope that we can all be part of creating the memory of the future!

Appendix A
Deposition Specifics

All devices were fabricated via physical vapor deposition(PVD), the machine used is located in the Gibbs' Lab at Northern Arizona University. Detailed instructions for use as well as specific parameters of use for this project can be found below.

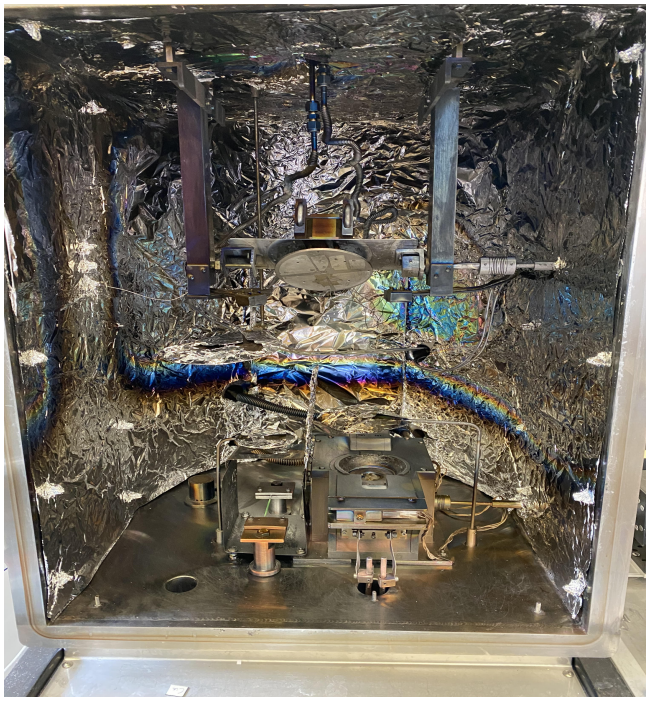


Figure 24: Deposition Chamber

The deposition system works as follows: First a material is loaded into the crucible chamber in the bottom left of the photo above. After adding the sample, the chamber is closed and pumped to a pressure in the 10^-6 Torr range. Next, an electron beam is generated and guided to hit the source material. The material then heats up to a vapor gas and floats to the top of the chamber subsequently growing a uniform thin film on the surface of the sample. For example, we will now deposit the bottom electrode (BE) nickel of 100 nm thickness on the silicon substrate. Then the sample is removed from the vacuum chamber and cleaned by the same process outlined before. In the case of the 20nm and 10nm "edgeless" samples, the WOx layer was deposited before it was removed from vacuum to ensure the interface between nickel and WOx is free from interface defects. For the edged devices, the shadow mask shown below is applied to the sample and the WOx and top electrode (TE) nickel is grown on the surface. For the edgeless devices, the shadow mask is applied to the sample on only the TE nickel is grown on the surface. The sample

is then removed from the vacuum chamber and the shadow mask is lifted off the surface by hand.

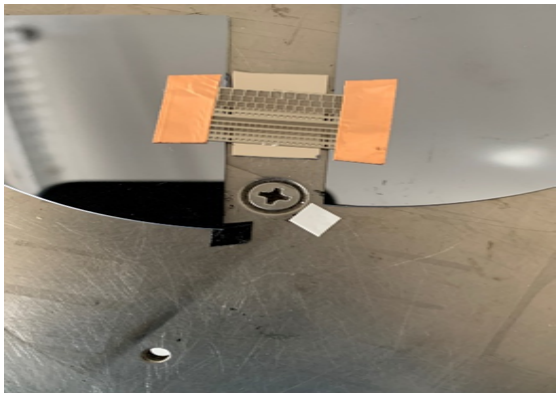


Figure 25: Shadow Mask Placement

Table Two: Vacuum Parameters

	100 nm	20 nm	10 nm
Vacuum Pressure (Torr)	$9*10^{-6}$ Torr	$6.61*10^{-6}$ Torr	$6.13*10^{-6}$ Torr
Deposition Rate (Angstrom per second)	0.1-0.6 (0.45 average)	0.1 - 0.8 (0.45 average)	0.1 - 0.6 (0.45 average)
Coil Voltage (kiloVolts)	6-6.62	6-6.3	6-6.5
Coil Current (Amp)	42.3	43.7	43.2
E-beam current (mA)	25mA	40mA	35mA

The parameters of deposition are shown in the table above. The parameters were all meant to be roughly the same except for the deposition pressure which was lowered for the 20nm and 10nm devices. As mentioned in the prototype section, an issue was found where the deposition rate of WOx was too fast to grow thin film reliability. So, I enlisted the help of Dr. Sumant Sarkar to figure out how to lower the deposition rate of transition metal oxides. The solution implemented was to lower the coil* voltage from 10,000 Volts to 6000 Volts, this lowered the kinetic energy of the electron beam and made the beam hit the edge of the material container rather than the center of the material. By slowly increasing the coil voltage in

increments of 0.01 kV I was able to keep the deposition rate somewhat constant. This lower deposition rate allowed me to fabricate the thin film devices reliably, as shown in the QCD thickness measurement shown in the photographs below (the Thick (kA) column shows the thickness in kilo-Angstroms).

Figure 26: PVD Deposition Rate

Appendix B
Optical Testing Additional Information

Testing Set Up:

After fabrication of WOx on ITO coated glass, place a sample into Jasco UV-Vis Spectrometer as shown in the system image page. Start device, purge chamber with Nitrogen gas for 5 minutes. Setup Spectrum analyzer to have a scan from 180 nm to 800nm wavelengths with a pitch of 0.1nm or 1nm. After adding the Indium Tin Oxide (ITO) top electrode, add a sample to the spectrometer but this time with the bulk ITO area in the laser target, purge with nitrogen gas. Immediately after, set the sample such that the targeted area is the device area with patterned electrodes. After this data is collected anneal the sample in the Air Furnace at 300 degrees C for 30 minutes., then perform the spectroscopy again on the bulk ITO area.

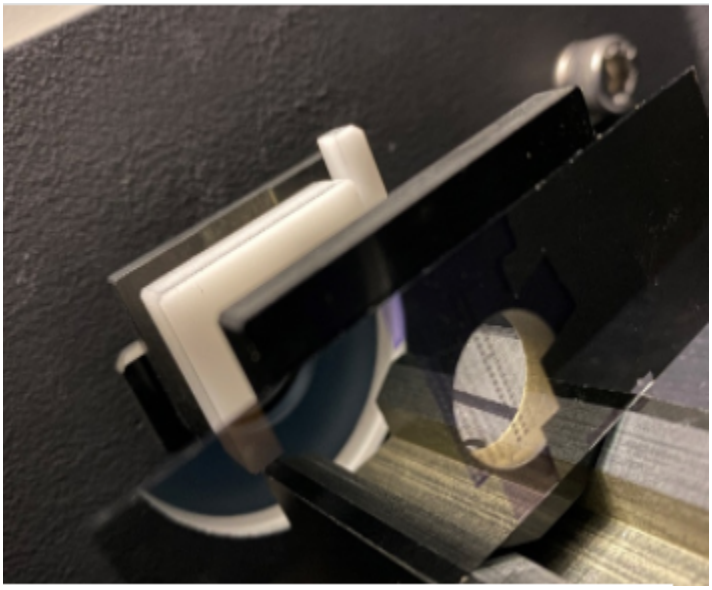


Figure 27: Set Up for Optical Testing of Jasco UV- Vis Spectrometer